

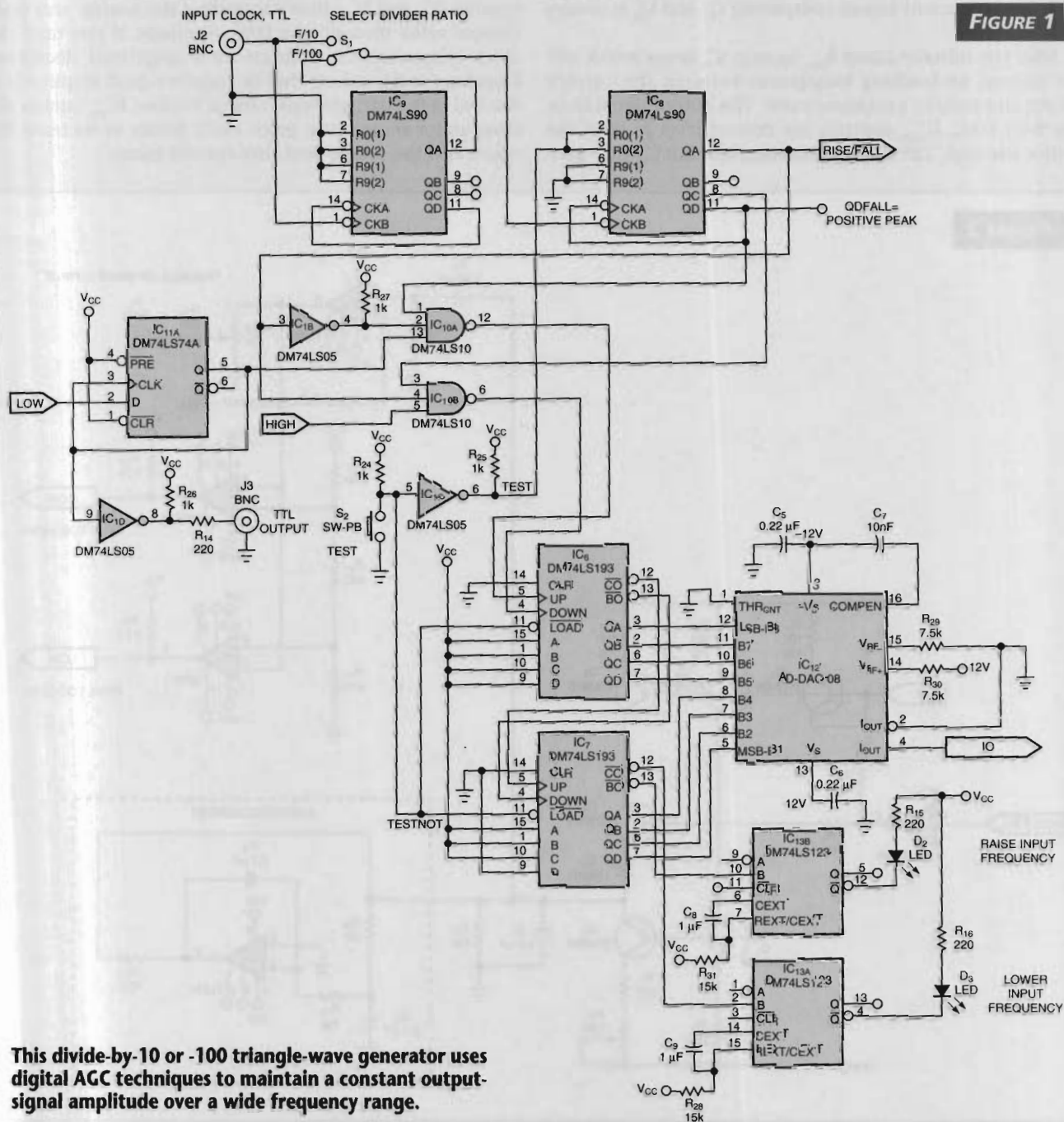
Scheme yields frequency-locked triangle waves

DANIEL DUFRESNE, DECATRON, ST BRUNO, PQ, CANADA

The circuit in Figures 1 and 2 generates frequency-locked triangle waves of constant amplitude. It uses readily available TTL and other older-technology parts. The circuit portion in

Figure 1 comprises the frequency dividers, counters, and converter. The portion in Figure 2 contains current sources, output circuits, and comparators. The circuit satisfies a need

FIGURE 1



This divide-by-10 or -100 triangle-wave generator uses digital AGC techniques to maintain a constant output-signal amplitude over a wide frequency range.

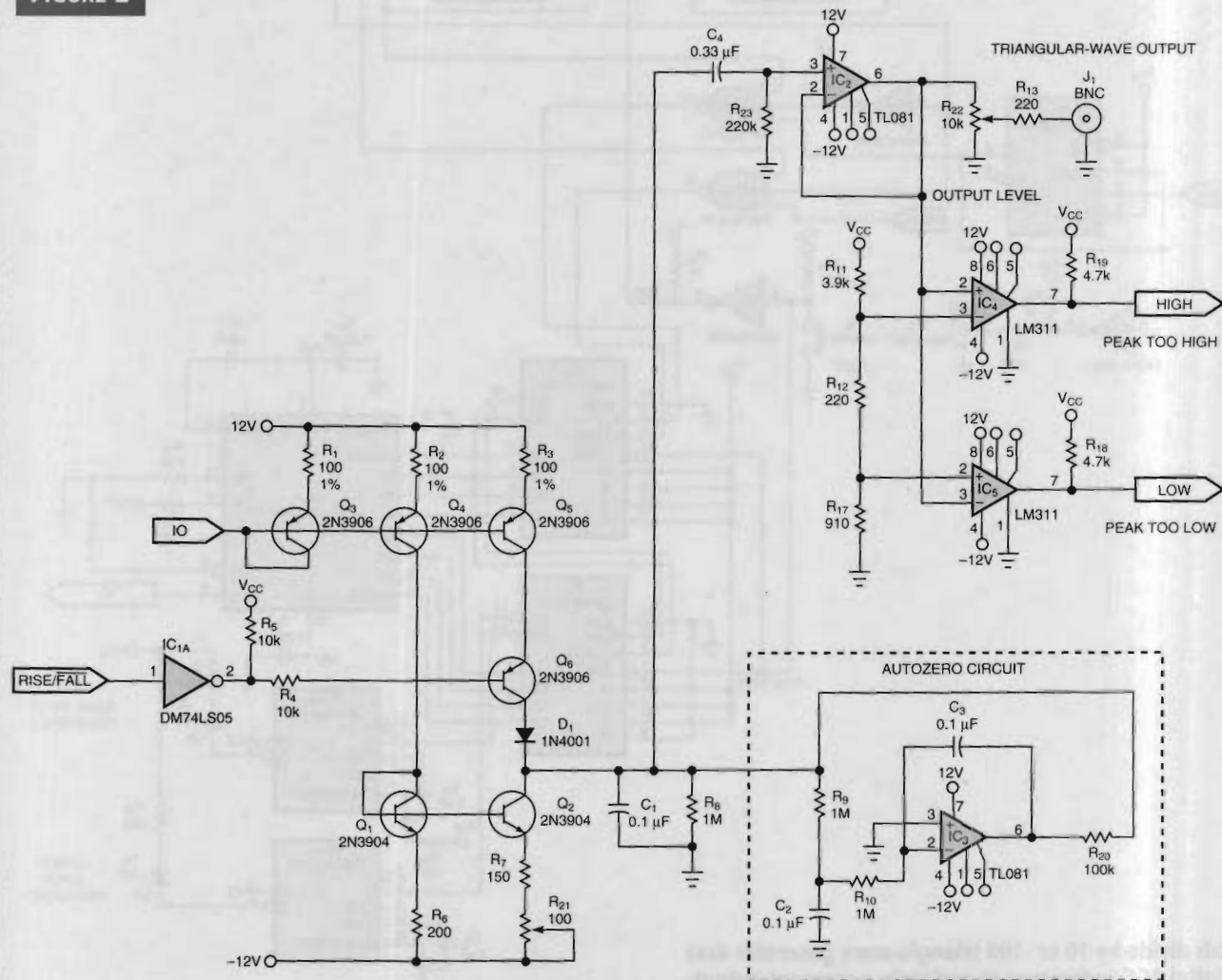
for a triangle wave of approximately constant amplitude, at a frequency exactly one-tenth or $1/100$ that of an input TTL clock. The input frequency can vary over a wide range before the circuit loses lock. The triangle-wave output frequency ranges from 250 Hz to 2.5 kHz. Two decade dividers divide the input clock by 10 or 100. Switch S_1 selects the divider ratio. The signal RISE/FALL is a 50%-duty-cycle wave that turns on a 2I current source, comprising transistors Q_3 , Q_4 , and Q_5 ; a -I current source comprising Q_1 and Q_2 is always on.

After you initially adjust R_{21} , op amp IC_3 keeps any dc offset (caused by tracking imbalances between the current source and sink) to a minimal value. The output signal from the 8-bit DAC, IC_{12} , controls the current level in both the source and sink. The currents sum on capacitor C_2 , thus gen-

erating a triangle wave. An op amp buffers the triangular signal; potentiometer R_{22} adjusts the output level. Assuming a fixed input frequency and a fixed capacitor value, you can adjust the current sources for the desired amplitude.

If the frequency decreases, the triangle-wave amplitude increases. To keep the amplitude constant, comparator IC_4 detects that the positive-peak amplitude is too high. The comparator sends input-clock signals to decrement the 8-bit counter IC_6 and IC_7 , thus controlling the source- and sink-current value through the DAC. Similarly, if you raise the clock frequency, the triangle-wave amplitude decreases. Comparator IC_5 detects that the positive-peak amplitude at the end of the triangle wave's rise is too low. IC_{11a} latches the comparator output and gates clock pulses to increase the count and the source- and sink-current values.

FIGURE 2



A companion to Figure 1's converter, this block contains the supporting current sources, output circuits, and comparators.

If you run out of counts on IC₆ and IC₇, the carry and borrow output signals trigger the monostables, IC_{13A} and IC_{13B}. LED D₂ or D₃ lights to warn you to change the input frequency accordingly. Frequency tracking is asymmetric: As soon as the circuit detects the high limit, pulses decrement the counter. The sooner the high limit occurs, the more decrementing pulses the counter receives. However, you detect that the current is too low only when the RISE/FALL signal falls, and the triangular wave is still below the positive-peak low limit. This occurrence triggers a single pulse.

To adjust the circuit, set the divider to $f/10$, apply a 10-kHz TTL signal to the clock input, short-circuit C₂, push the TEST button, and adjust R₂₂ for a zero-centered triangular wave. Release the TEST button, and remove the short circuit. You can increase the frequency range by using a bigger counter and a higher resolution DAC or by band-switching the current-summing capacitor, C₁, with some added logic that the borrow and carry outputs of IC₇ trigger. (DI #2127) 

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Off-the-shelf MMIC suits mixer applications

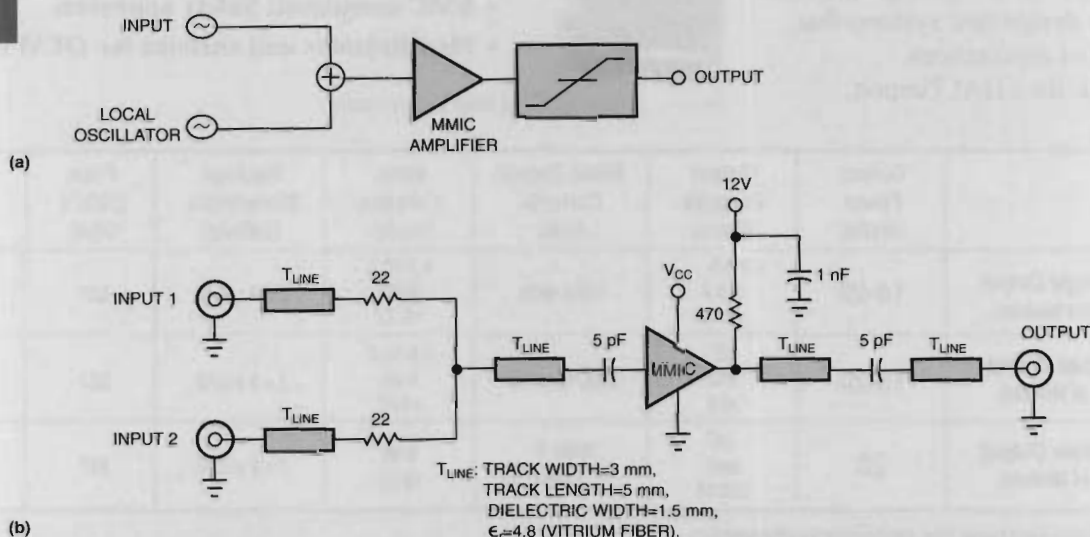
J LEIRA PAZ, M PEREIRA VARELA, AND FP FONTAN, UNIVERSITY OF VIGO, SPAIN

You can use a standard monolithic-microwave IC (MMIC) to configure an efficient and economical microwave mixer. Some systems require a mixer with an input level lower than -10 dBm. Many available mixers, however, require greater than 10-dBm input power. The circuit in Figure 1 exploits the inherent nonlinearity of a Mini-Circuits (Brooklyn, NY) MAR6 microwave amplifier to configure a low-level mixer. The idea is to add the input signals and feed the sum to the MMIC (Figure 1a). The amplifier's saturation characteristic produces the harmonics and intermodulation products. The MMIC has greater than 10-dB gain at frequencies over 1 GHz, a desirable characteristic for making mixers for the 0.9, 1.8-, and 2.5-GHz bands.

The MMIC also has a maximum power output of 2 dBm

at 1-dB compression, a useful trait for obtaining intermodulation products with low input power. The gain of the MMIC varies from 17 dB at 100 MHz to 10 dB at 2.4 GHz. The gain can thus generate intermodulation products using two input signals whose power is lower than -10 dBm. Finally, the MMIC's 3-dB noise figure is an important factor for low-level input signals. The adder uses two standard-value 22Ω resistors and thus presents a reasonably good impedance match in 50Ω systems (Figure 1b). For perfect impedance matching, you would need 20.7Ω (unavailable) resistors. With the 22Ω resistors, the input VSWR is less than 1.4 at 1 GHz. To obtain optimum results, you should use microstrip techniques, with the dimensions in Figure 1b, in designing the pc board.

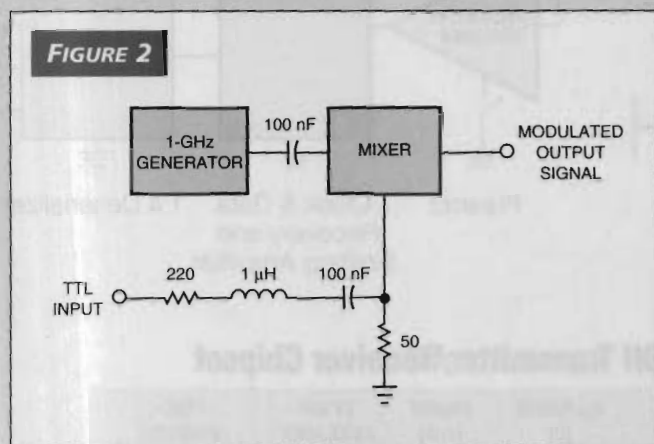
FIGURE 1



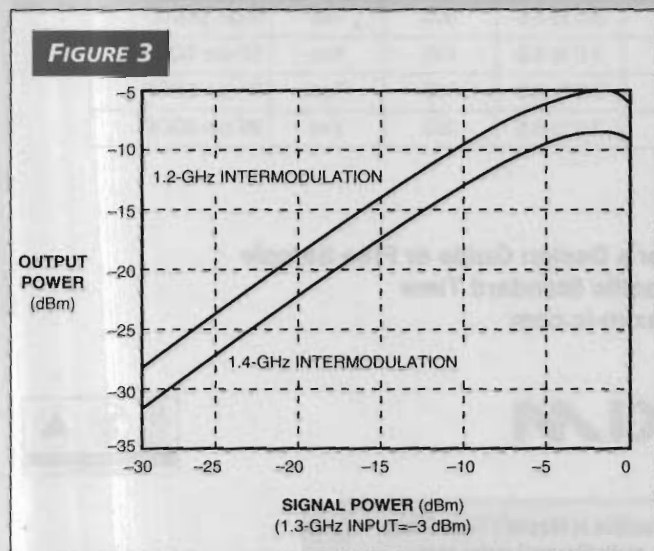
A summing network and a standard MMIC (a), connected with microstrip techniques (b), produce an efficient mixer for low-level signals.

You can use this mixer in a variety of applications: down-converters and modulators, for example. Another example is an amplitude-shift-keying (ASK) modulator for digital applications (Figure 2). The mixer block in Figure 2 uses the circuit in Figure 1a. The measurements of Figures 3, 4, and 5 reflect a 1-GHz carrier frequency and a 4-Mbps digital signal. To obtain a good relationship between the carrier level and the modulated-signal level, use a -5-dBm input-carrier level, a ± 0.5 -dBm digital signal, and a 12V supply. The output-signal level is 0 dBm.

Figure 3 shows the magnitude of the intermodulation products as a function of the 100-MHz signal power. The input frequencies are 1.3 GHz and 100 MHz. The most important intermodulation frequencies are the sum-and-dif-



The circuit in Figure 1b is the mixer block in this 1-GHz ASK modulator.

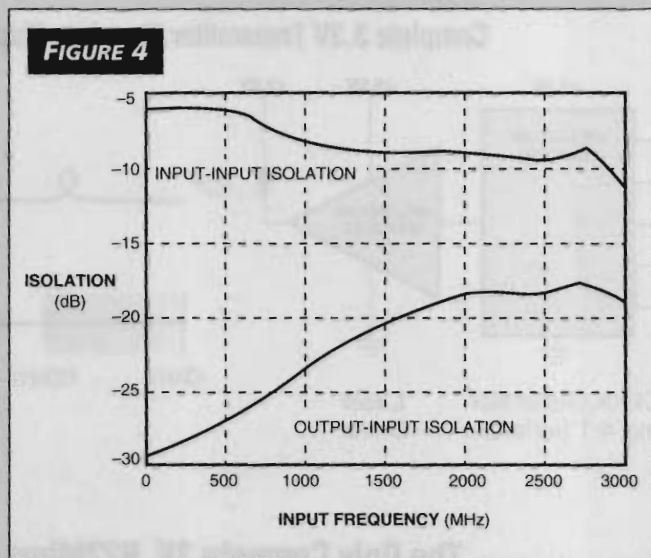


The output levels of the sum-and-difference intermodulation products in Figure 2's circuit vary linearly with the 100-MHz signal power.

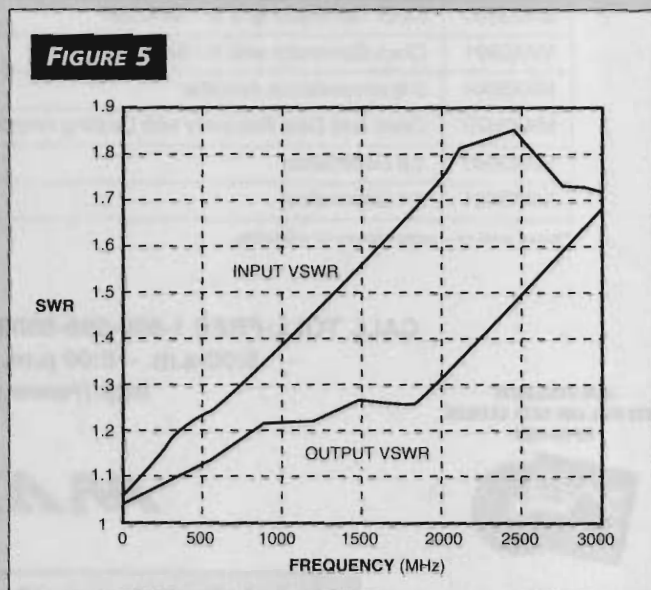
ference intermodulation products, 1.2 and 1.4 GHz. Figure 4 shows the input-input and output-input isolation characteristics. Figure 5 gives the variation of the input and output VSWR as a function of the input frequency. (DI #2136)

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Input-input isolation for Figure 2's circuit improves with increasing input frequency; output-input isolation degrades but remains reasonably high to 3 GHz.



The slight input-impedance mismatch and varying input reactance of the MMIC produces input VSWR degradation with frequency, but the VSWR remains within a respectable 1.4 at frequencies to 1 GHz.

of the nonzero output of IC₁, but also compensates for any residual offsets. You achieve a full-scale output of 100 mV using the 100% adjustment.

The circuit draws 2.56 mA, which, if battery-powered, results in a battery life of about 250 hours. You can drop the total consumption to approximately 625 μ A by changing IC₂ and IC₃ to LT1078s and by powering IC₁ from the 5V output

of the LT1121-5. This change lengthens battery life to more than 1000 hours. However, these changes also reduce the overall accuracy of the circuit and prevent IC₃ from driving anything but very light capacitive loads, such as high-impedance ADC inputs. (DI #2145) 

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Vital-signs monitor consumes less than 50 μ A

LEONARD SCHUPAK, DISCOVISION ASSOCIATES, IRVINE, CA

A remote data-acquisition circuit for monitoring a patient's vital signs—pulse rate, respiration, and temperature—uses very little power as well as inexpensive sensors and circuits (Figure 1). The data-acquisition portion uses the low-cost CD4000 series of CMOS ICs and consumes less than 50 μ A from a 3V battery. The circuit uses 50 $\times$ oversampled sigma-delta ADCs with a PWM/FM system, which combines three data channels on one RF carrier.

In Figure 1, the pulse sensor comprises a pair of conductive plastic electrodes that monitor two EKG lead points across the patient's chest. These electrodes are similar to those used on a popular and effective pulse monitor for athletic activities. The respiration sensor is an Amp (Harrisburg, PA) DT1-028K, which consists of a piezoelectric-film element mounted on a flexible beam that attaches with a chest strap similar to the same athletic monitor. The strap uses the beam as one of its suspension loops, the electronics assembly attaches to the other end, and the complete assembly straps to the patient's chest. The temperature sensor comprises a 50-k Ω thermistor and linearizing resistor mounted in the EKG electrode, which makes a good thermal connection to the patient's body.

Using the unique properties of the CD4069 as an analog component, the circuit implements two second-order sigma-delta ADCs that sample the ac components of the pulse (EKG) and respiration at a nominal 2-kHz clock rate. The circuit develops this clock using the thermistor as a tuning element in a temperature-to-frequency converter. Temperature is a very low-frequency (essentially dc) data-channel component, and pulse and respiration are higher frequency ac. Thus, you can easily combine all three channels in one serial data channel for transmission over the RF link.

The analog circuit also includes an open-lead detector that rings an alarm if the EKG lead loses contact. IC_{1C} and IC_{1F} form a Schmitt trigger that disables the RF-carrier output when the sense of skin conductivity is lost.

IC_{2A} and IC_{2D} form a straightforward clock oscillator. Although easy to design, this oscillator imposes some inter-

esting calibration problems in operation. The thermistor, R₁, and tuning capacitor, C₁, determine the frequency. For a thermistor of 11 k Ω at 98.6°F, C₁ should be 0.022 μ F for a clock frequency of 2 kHz. Connecting these components to IC_{2A} and IC_{2D}, as the figure shows, provides a convenient pc-board layout with good isolation from these low-level input signals. You can use an additional resistor set to optimize the frequency range, depending on the thermistor selection. The operator usually performs a calibration cycle when you apply the unit to the patient, setting the "current reading" to a known temperature obtained directly from the patient.

The operation of the ADC is straightforward but has some unusual aspects. (Note that because of the way the CD4069 inverter works—used here exclusively for analog-amplifier functions—the figure uses a one-input NAND gate as the logic symbol to differentiate from the triangle symbol.) An ADC channel comprises three CD4069 inverters in series, for which two operate as analog integrating amplifiers biased in the linear region. In this configuration, each CD4069 section yields about 30 dB of gain and a bandwidth in excess of 2 kHz. The third inverter and flip-flop input act as the typical comparator part of the ADC.

The first stage is a relatively uncomplicated integrator with an indeterminate time constant of approximately 1 to 10 μ sec. The second stage has a pole/zero response that flattens to -20 dB at approximately 5 kHz. Feedback from the sampling register (flip-flop) provides a stable, wideband

TABLE 1—PHASE INCREMENTS

Channel A	Channel B	Phase increment (°)
0	0	45
0	1	90
1	0	135
1	1	180

Signal conditioning precisely indicates humidity

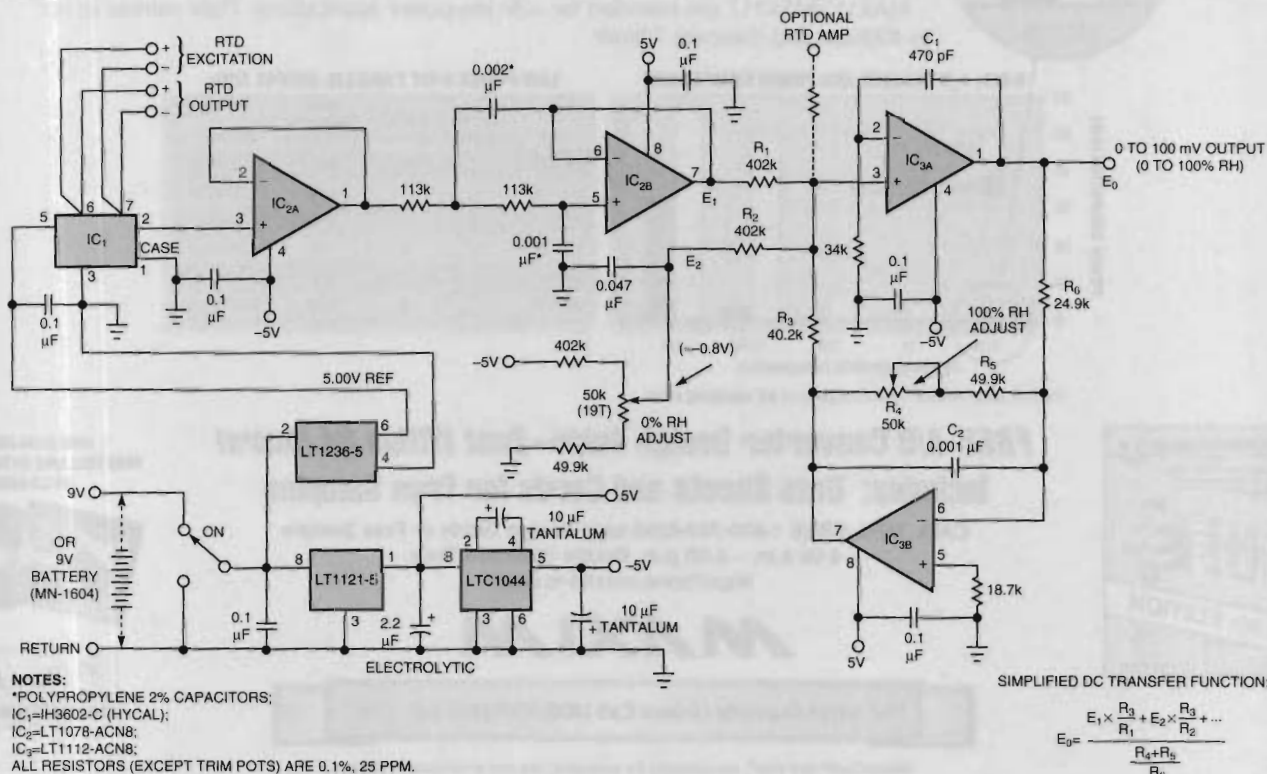
WILLIAM WHITEHEAD, LAFAYETTE, CO

The circuit in **Figure 1** translates the level of humidity from 0 to 100% into a stable, respective dc signal of 0 to 100 mV. The heart of the circuit is IC₁, the IH3602-C relative-humidity sensor (Microswitch/HyCal Sensing Products, Freeport, IL). This device operates on 5V at 200 μ A and provides a dc output of 0.8 to 4.0V over the 0 to 100% humidity range. The output impedance is 5 μ A when sourcing, and on-chip circuitry preconditions the humidity-related charge of a thermoset polymer dielectric capacitor. The dc output contains a small amount of 1-kHz modulation, which is an artifact of typical switched-capacitor circuits. Device accuracy is $\pm 2\%$ relative humidity, and linearity is $\pm 0.5\%$. The six-pin TO-5 package includes a precision thin-film, 1-k Ω RTD that you can use in applications that require temperature-corrected relative-humidity data.

The LT1236-5 provides a stable 5V supply for IC₁, which precludes any ratiometric changes in the sensor's output that would otherwise occur with less stable 5V supplies. Amplifier IC_{2A}'s voltage follower buffers the sensor's high-impedance output. IC_{2B}, a 1-kHz, two-pole Butterworth filter, reduces the 1-kHz chopper modulation. The unique output stage comprising IC₃ is a precise, dc-accurate, ultralinear, noninverting summing/scaling amplifier. The LT1112 performs well for this function because it has high large-signal gain (A_{VOL}), low input bias current (I_B), and low input offset voltage (V_{OS}). The summing node of IC_{3A} is a handy spot to add a temperature-correcting term, as the **figure** indicates. C₁ and C₂ roll off any high-frequency gain/phase-related oscillations.

The 0% relative-humidity adjustment not only takes care

FIGURE 1



Precise signal conditioning transforms the 0.8 to 4.0V output of an accurate 0 to 100% relative-humidity sensor, IC₁, to a 0 to 100-mV output.

inner loop as well as the main outer loop. The 100-M Ω resistors in the feedback loops are readily available from several vendors in surface-mount configuration and are reliable when you use good assembly practices.

The components in the figure comprise only the front-end input portion of the design; the noise filter and subsequent decoder/application circuits reside at the receiver. Before transmission, the circuit combines the three channels of data into one modulating signal using a PCM format similar to modified FM (MFM) for which the temperature-controlled clock oscillator determines the pulse-rate clock. In other words, the transmitter uses a complex set of modulating codes that include a PCM/FM component superimposed on an amplitude-shift-keyed (ASK) carrier. The temperature-sensitive oscillator frequency varies about 20% total over the expected range of body temperatures, and this

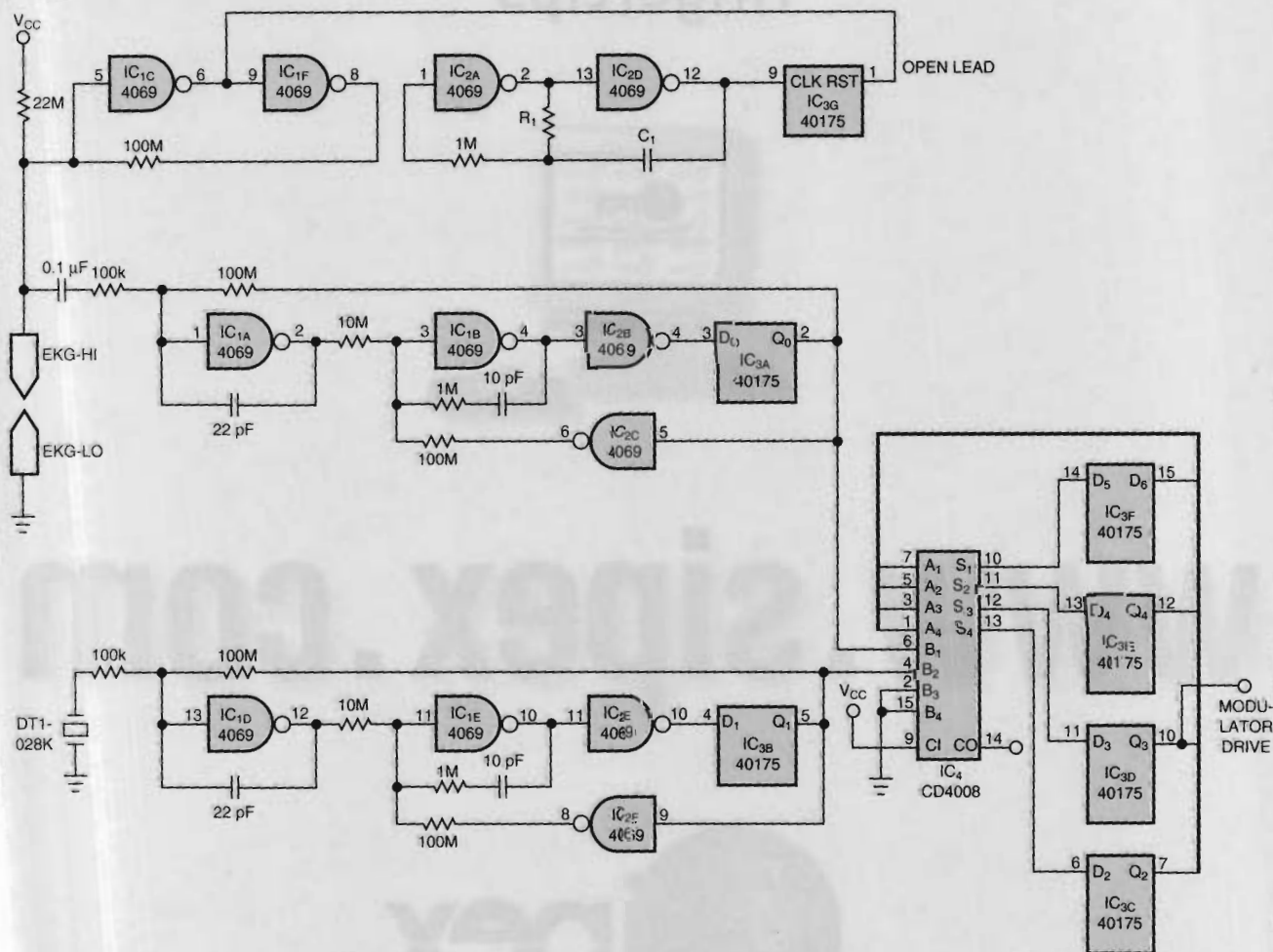
variable rate is adequate to transmit the digital PCM data.

A CD4008 full adder encodes the digital data from each ADC flip-flop in MFM form. A simple 3-bit digital synthesizer accomplishes the encoding; the contents of output registers IC_{3C} and IC_{3D} determine the output phase. The ADC's data contents determine the incremental phase change at each clock (Table 1). The circuit then uses the most significant bit of the output register as the ASK signal. The 4-bit register then stores the sum of the data, or the phase increment with the current contents, representing the digital phase of the modulation carrier. The maximum resulting fundamental frequency of this carrier is then one-half the clock frequency. (DI #2149)

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FIGURE 1



Inexpensive sensors and simple CD4069-based sigma-delta ADCs comprise the front end of low-power, remote data-acquisition for monitoring a patient's temperature, pulse, and respiration.

Optocoupled gate detects motor operation

JIM KNIPFER, LIEBEL-FLARSHEIM CO, CINCINNATI, OH

Most applications require redundant system checks to ensure that devices are operating as expected. The circuit in Figure 1 detects when a PWM-controlled servo motor is running. You can monitor the motor-running signal output with a CPU or tie the output to hardware that indicates a fault if the motor is running when it should be off. The motor's output connects to input resistors R_{IN1} and R_{IN2} . The use of two resistors protects the motor or servo amplifier in the case of a short circuit. R_{IN1} and R_{IN2} also serve as current-limiting resistors for the LED in the opto gate, IC_2 .

The value of R_{IN1} and R_{IN2} in Figure 1 is suitable for 150V nominal servo output voltage. Because the input voltage can reverse, the circuit uses a full-wave bridge (D_1 to D_4) before the input of the opto-gate IC. The circuit needs a high-speed opto gate, because when the motor runs at low speeds, the servo-output duty cycle can be only a fractional percentage, thereby providing only 1- μ sec or narrower pulses to sample.

TABLE 1—APPROXIMATE TIME-OUT PERIODS

A	B	Approximate time-out period
0	0	350 msec
0	1	45 msec
1	0	10 msec
1	1	2.8 sec

When no signal is present at the input resistors, the output of the opto gate is high, causing the output of inverter IC_3 to be low. The low output allows the MC14541 counter, IC_1 , to count at the frequency determined by R_1 , R_2 , and C_1 .

You can determine the time-out by multiplying the count range (selected by inputs A and B) by the period of the frequency set in IC_1 . Table 1 shows approximate time-outs. Upon the initial application of power, the motor-running signal remains active until the time-out occurs.

Upon detection of a servo pulse of 500 nsec or longer, the master reset pin (Pin 6 of IC_1) goes high, resets the internal counter, and asserts the motor-running signal. The motor-running signal remains low for the amount of time shown in Table 1. The time-out for the circuit in Figure 1 is approximately 10 msec. (DI #2155)

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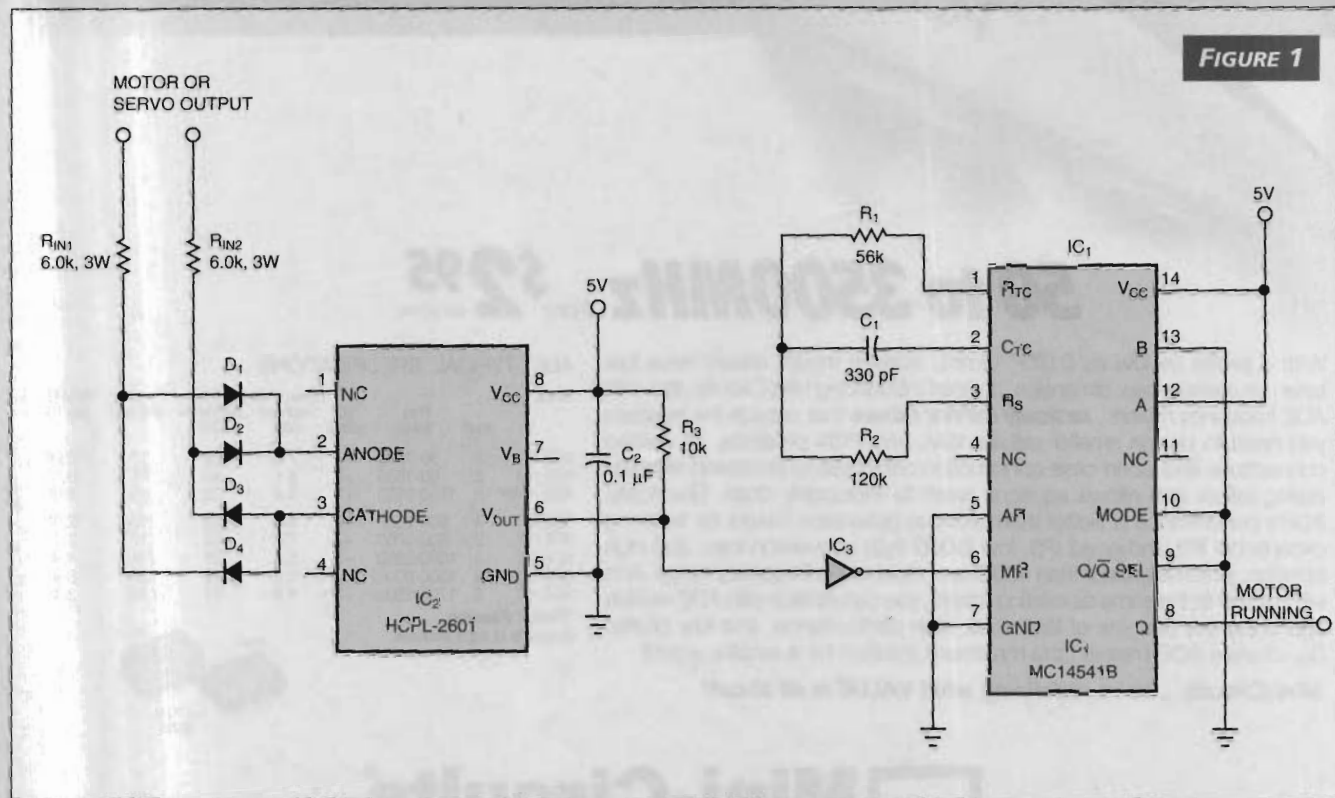


FIGURE 1

Did you leave your motor running? This circuit lets you or your μ C know.